REMARKS

Claims 1-13 are pending. Claims 6-11 have been withdrawn. Reconsideration and allowance based on the below comments are respectfully requested.

Applicants appreciate the indication that claims 2-5 as containing allowable subject matter.

Applicants hereby incorporate the arguments filed in the Reply dated February 25, 2005. Further arguments are provided below to elucidate embodiments of the present invention and the distinction from the teachings of the cited prior art.

Prior Art Rejection

The Office Action rejects claims 1 and 13 under 35 U.S.C. §103(a) as being unpatentable over Kuroda (US 5,487,029) in view of Clemons (US 4,599,709); claim 12 under 35 U.S.C. §103(a) as being unpatentable over Kuroda in view of Clemons and Seyyedy (US 5,969,380). These rejections are respectfully traversed.

Applicants respectfully submit that one of ordinary skill in the art would not look to the teachings of Clemons to provide the claimed passive matrix addressable ferroelectric memory claimed by applicants in independent claims 1, 12 and 13. Applicants respectfully submit that Clemons teaches an SRAM (static random access memory) which, as discussed below, is very different from the passive matrix addressable ferroelectric memory.

A static RAM stores data in memory cells based on flip-flops and retains the memory cells as long as the power is on. When the power is turned off, the stored data is lost. DRAM (dynamic random access memory) are based on memory cells with transistor switches and a capacitor for storing the data. The capacitor charge is lost over time and therefore the data will be lost unless the dynamic RAM is regularly refreshed or rewritten with the same data originally stored therein. In both static RAM and dynamic RAM, the random access time is short, usually a small fraction of a microsecond. Further, the dynamic RAM or S-RAM when implemented on a single memory chip usually has a limited storage capacity for instance, a range of a half megabyte to possibly as much as a quarter of a gigabyte. A fast random access time then usually

requires a fairly small read/write parallel access, e.g., limited to byte-wise read/write, i.e., in groups of 4, 8, 16 or 32 bits at a time.

As discussed in Clemons, one disadvantage with the prior art was parallel access was divided over a number of groups of bit lines and therefore in order to access the byte simultaneously, the correct bit line in each group would have to be connected to a single sense amplifier provided for that group of bit lines and the byte read out in parallel accessing all groups. For example, for a four bit word, four groups would have to be accessed. In response to this problem, Clemons proposes to divide this bit line in byte blocks such that, for example, four bit lines corresponds to a single byte block and hence a byte can be stored in this block and read out to the I/O line to which there maybe attached a sensed amplifier. As compared with the prior art, Clemons offers the improvement of parallel byte wise read out, as all bit lines of a byte block can be connected with respective I/O lines.

Further, Clemons teaches there shall be appropriate block decoders coordinated with pass-gate means, for instance, transistors. The pass-gate served to switch the bit lines onto the I/O lines. As shown in Fig. 2, there would be at least one spare line for each byte block. The problem solved by Clemons is exclusively connected with static RAM which are made with flip-flops and allow for a parallel readout of a byte by simply accessing all memory cells in a single byte block.

In contrast, the present invention is not at all concerned with random access memories, but to the contrary addresses concerns regarding non-volatile passive matrix addressable ferroelectric memories. The passive matrix addressable ferroelectric memory currently stores data as polarization values in ferroelectric capacitors that are continuously in ohmic contact with access electrodes. The access electrodes correspond to the word and bit lines, and retain indefinitely the polarization state of the memory cell even when the power is switched off. In contrast with a RAM, a ferroelectric memory has some orders of magnitude slower random access times, but this more than offset by ferroelectric memory usually being adapted for parallel readout of huge data words running into the size of several thousand bits. In a passive matrix addressable memory array, the ferroelectric capacitors forming the memory cells are defined in

memory material provided between respectively a first set of electrodes called word lines, a second set of electrodes call bit lines where the electrodes are first set are usually orientated orthogonal to electrodes of a second set. A parallel write and read in such a memory involves access in all memory cells on a single word line called the active word line and then reading the data on all memory cells on this word line and parallel via the bit lines of the array, each bit line being connected with a sense amplifier.

In a passive matrix addressable ferroelectric memory, there is no need for a larger number of sense amplifiers and the specific number of bit spots that shall be accessed to a single readout operation. Thus, according to embodiments of the present invention the word lines are segmented to correspond with a number of parallel readable memory cells, i.e., a similar number of bit lines arranged side by side in each segment, such that the number of sense amplifiers consequently are limited to the number of bit lines in a single segment. Moreover, in addition to reducing power consumption and saving real estate on a chip due to the lower number of sense amplifiers, the effect or voltage disturbs may also be reduced since a lower number of memory cells are accessed simultaneously and generally the power consumption is reduced.

While the prior art as relevant in the present invention would be one sense amplifier for each bit line of a passive matrix or array, this contrasts with prior art S-RAMS where a single sense amplifier is connectable with each group of bits lines. With four-bit line groups a byte could then read by reading in parallel one bit line from each group connected to the appropriate sense amplifier. Clemons proposes instead that a byte is read in parallel from the byte block consisting of adjacent bit lines similar to the present invention, but of course the number of sense amplifiers are the same as before, i.e., unchanged. Hence, Clemons neither addresses nor solves the problem posed by the embodiments of the present invention and while the number of sense amplifiers is reduced in the embodiments of the present invention, the device according to Clemons has exactly the same number of sense amplifiers as used in the prior art.

Regarding the skill factor illustrated in Clemons, Clemons teaches the static RAM with small data words, typically four bit or eight bit data words, which is typical for the time period of the Clemons reference (1984), Clemons memory would probably have been adapted to store 64

kilobits and eight bit words. In contrast, the present invention is concerned with parallel readout or data words running into said kilobits in order, for example, to compensate for the slow random access time as compared with either a static RAM or dynamic RAM.

As illustrated above, although there are some similarities with how the static RAM of Clemons is illustrated with regard to embodiments of the present invention, applicants respectfully submit that a static RAM does not function the same as a passive matrix addressable ferroelectric memory and in fact, displays quite different characteristics. Therefore, one of ordinary skill in the art would not look to the teachings of a static RAM to provide a passive matrix addressable ferroelectric memory, let alone the device characteristics of a passive matrix addressable ferroelectric memory, as recited in independent claims 1, 12 and 13.

Thus, applicants respectfully submit that Clemons fails to teach the features of independent claims 1, 12 and 13 for which it is applied. Specifically, Clemons fails to teach or suggest, *inter alia*, the word lines are divided into a number of segments, each segment including and being defined by a plurality of adjoining bit lines in the matrix, each word line in a segment is differentiated based on the position of the word line within the segment, each word line in the segment being adjoined to a separate bit line, where each separate bit line assigned to a segment is connected with an associated sensing means, such, that the word line of the same position within each segment is sensed at the associated sensing means, thus enabling simultaneous connection of all memory cells assigned to a word line on a segment for readout via the corresponding bit lines of the segment, as recited in independent claims 1, 12 and 13.

Further, Clemons fails to teach or suggest, *inter alia*, a number of sensing devices connected to each of the corresponding bit lines within each segment of word lines, where each word line and each segment is differentiated based on the position of the word line within the segment, each word line and each segment being adjoined to a separate bit line, such that the word line of the same position within each segment is sensed and an associated sensing device from the number of sensing devices, thus enabling simultaneous connection of all memory cells assigned to a segment, as recited in claim 13.

Further, Kuroda and Seyyedy fail to make up for the deficiencies of Clemons. Accordingly, reconsideration and withdrawal of the rejections are respectfully requested. Applicants respectfully submit that claims 1, 12 and 13 are in condition for allowance. Claims 1 and 12 are generic claims to the alleged species defined by claims 2-5 and claims 6-9. Applicants request reconsideration of the un-elected species represented by claims 6-9. Accordingly, applicants respectfully request the allowance of claims 1-9, 12 and 13 in the application.

Conclusion

For at least these reasons, it is respectfully submitted that claims 1-9, 12 and 13 are distinguishable over the cited art. Favorable consideration and prompt allowance are earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Chad J. BIllings (Reg. No. 48,917) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

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Respectfully submitted,

By #39,491

Michael K. Mutter
Registration No.: 29,680
BIRCH, STEWART, KOLASCH & BIRCH, LLP
8110 Gatehouse Rd., Suite 100 East
P.O. Box 747
Falls Church, Virginia 22040-0747
(703) 205-8000
Attorney for Applicant